LISTING OF CLAIMS

This Listing of Claims replaces all prior versions and listings of claims in this application.

Claims 1-29 (canceled)

30. (New) A method of arranging an on-chip capacitor on a chip to create a capacitance between a first conducting connection point in a first plane of the chip and a second conducting connection point in a second plane of the chip, comprising the steps of:

creating at least one conducting extension of a first type from the first conducting connection point toward the second plane to a third plane, and

creating at least one conducting extension of a second type from the second conducting connection point toward the first plane to a fourth plane,

wherein the fourth plane is located between the first plane and the second plane, the third plane is located between the fourth plane and the second plane, and the conducting extension of the first type is isolated from the conducting extension of the second type by a dielectric allowing an electric field to be created between the conducting extensions.

31. (New) The method of claim 30, wherein a plurality of conducting extensions of the first type are created.

32. (New) The method of claim 30, wherein a plurality of conducting extensions of the second type are created.

33. (New) The method of claim 30, wherein the first plane is a side of a first metal layer, the second plane is a side of a second metal layer, and the first and second metal layers are different metal layers.

34. (New) The method of claim 33, wherein the third and fourth planes are different sides of a third metal layer.

35. (New) The method of claim 33, wherein the third plane is a side of a third metal layer, the fourth plane is a side of a fourth metal layer, and the third and fourth metal layers are different metal layers.

36. (New) The method of claim 30, wherein the at least one conducting extension of the first type originates in a metal layer and terminates in a metal layer.

37. (New) The method of claim 36, wherein the at least one conducting extension of the first type extends through at least one further metal layer.

38. (New) The method of claim 30, wherein the at least one conducting extension of the second type originates in a metal layer and terminates in a metal layer.

39. (New) The method of claim 38, wherein the at least one conducting extension of the second type extends through at least one further metal layer.

40. (New) The method of claim 30, further comprising the step of extending the first conducting connection point in the first plane of the chip such that the first conducting connection point comprises a conducting plate.

41. (New) The method of claim 30, further comprising the step of extending the second conducting connection point in the second plane of the chip such that the second conducting connection point comprises a conducting plate.

42. (New) The method of claim 30, further comprising the step of arranging one or more on-chip capacitors with at least one other passive component into an on-chip resonant circuit.

43. (New) The method of claim 30, further comprising the step of arranging one or more on-chip capacitors into an on-chip transmission line.

44. (New) An on-chip capacitor with a capacitance between a first conducting connection point in a first plane of a chip and a second conducting connection point in a second plane of the chip, the on-chip capacitor comprising:

at least one conducting extension of a first type extending from the first conducting connection point toward the second plane to a third plane, and

at least one conducting extension of a second type extending from the second conducting connection point toward the first plane to a fourth plane,

wherein the fourth plane is located between the first plane and the second plane, the third plane is located between the fourth plane and the second plane, and the conducting extension of the first type is isolated from the conducting extension of the

second type by a dielectric allowing an electrical field to be created between the extensions.

45. (New) The on-chip capacitor of claim 44, wherein the on-chip capacitor comprises a plurality of conducting extensions of the first type.

46. (New) The on-chip capacitor of claim 44, wherein the on-chip capacitor comprises a plurality of conducting extensions of the second type.

47. (New) The on-chip capacitor of claim 44, wherein the first plane is a side of a first metal layer, the second plane is a side of a second metal layer, and the first and second metal layers are different metal layers.

48. (New) The on-chip capacitor of claim 47, wherein the third and fourth planes are different sides of a third metal layer.

49. (New) The on-chip capacitor of claim 47, wherein the third plane is a side of a third metal layer, the fourth plane is a side of a fourth metal layer, and the third and the fourth metal layers are different metal layers.

50. (New) The on-chip capacitor of claim 44, wherein the at least one conducting extension of the first type originates in a metal layer and terminates in a metal layer.

51. (New) The on-chip capacitor of claim 50, wherein the at least one conducting extension of the first type extends through at least one further metal layer.

52. (New) The on-chip capacitor of claim 44, wherein the at least one conducting extension of the second type originates in a metal layer and terminates in a metal layer.

53. (New) The on-chip capacitor of claim 52, wherein the at least one conducting extension of the second type extends through at least one further metal layer.

54. (New) The on-chip capacitor of claim 44, wherein the first conducting connection point in the first plane of the chip comprises a conducting plate.

55. (New) The on-chip capacitor of claim 44, wherein the second conducting connection point in the second plane of the chip comprises a conducting plate.

56. (New) The on-chip capacitor of claim 44, wherein the on-chip capacitor is included in a resonant circuit.

57. (New) An on-chip transmission line, wherein the transmission line comprises at least one on-chip capacitor defined by claim 44.

58. (New) The on-chip transmission line of claim 57, wherein the on-chip transmission line is included in a resonator, matching network, or power splitter.